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To: Assistant Commissioner for Patents
Box Patent Application
Washington D.C., 20231

Dear Sir:

Transmitted herewith for filing under 37 C.F.R. 1.53(b) is a:

☒ New Nonprovisional Utility Patent Application; or

☐ Continuation; or ☐ Divisional; or ☐ Continuation-In-Part (CIP); of prior US Application No. _____, filed on _____, having U.S. Examiner _____, in Group Art Unit _____

Of: Cynthia L. Recker and Patrick G. Drennan

For: **MISMATCH MODELING TOOL**

☒ 9 sheets of **FORMAL** drawings and 37 pages of specification and claims.

☒ Oath or declaration combined with Power of Attorney on 2 pages.

☐ Copy of oath or declaration from prior U.S. application serial no. _____
☐ The following named inventor(s) from the prior application are hereby deleted from this application in accordance with 37 C.F.R. 1.63(d)(2) and 1.33(b): _____.

☐ Foreign priority to EPO patent application having serial number _____ and a filing date of _____, is hereby claimed under 35 USC 119.

☒ An Assignment Transmittal Letter and Assignment of the invention to Motorola, Inc.

☒ An Information Disclosure Statement (IDS), with PTO-1449, and 2 citation copies.

☒ Return Receipt Postcard.

☐ Preliminary Amendment.

☐ Please cancel pending claims _____.

☐ Incorporation by Reference (for Continuation/Division/CIP application). The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein. Since the present application is based on a prior US application, please amend the specification by adding the following sentence before the first sentence of the specification:

"The present application is based on prior US application No. _____, filed on_____ _____, which is hereby incorporated by reference, and priority thereto for common subject matter is hereby claimed."

☐ Applicant hereby petitions pursuant to 37 C.F.R. §1.136(a) for a _____ month extension of time for response to the outstanding Official Action mailed _____. The period for response was previously set to elapse _____, and is accordingly hereby extended to _____, which is still within the six-month statutory period for response (35 U.S.C. § 133) which elapses _____. The reason for this petition is that a Division, Continuation, or CIP is being filed, and it is desired to maintain the present application in pending condition pursuant to 35 USC § 120 through at least the filing of the Division, Continuation, or CIP application. The required Extension Fee established by 37 C.F.R. § 1.17(a) pursuant to 35 U.S.C. § 41(a) (8) is:

EXTENSION	FEE
☐ First Month	$110.00
☐ Second Month	$380.00
☐ Third Month	$870.00
☐ Fourth Month	$1,360.00
☐ Fifth Month	$1,850.00

☒ The filing fee is calculated as follows:

CLAIMS AS FILED, LESS ANY CANCELED BY AMENDMENT

FOR	NUMBER OF CLAIMS	NUMBER EXTRA	RATE	FEE
TOTAL CLAIMS	20 - 20 =	0	x $18	= $0.00
INDEPENDENT CLAIMS	2 - 3 =	0	x $78	= $ 0.00
MULTIPLE DEPENDENT CLAIMS			$260	= $ 0.00
BASIC FEE				= $ 690.00
TOTAL FILING FEE				= $690.00

☒ Please charge Deposit Account No. 13-4771 in the amount of $ 690.00 for the Total Filing Fee, and the Extension Fee under 37 C.F.R. §1.136(a), if applicable.

☒ The Commissioner is hereby authorized to charge any additional fees which may be required now or in the future during the entire pendency of this application under 37 C.F.R. 1.16 or 37 C.F.R. 1.17, including any present or future time extension fees which may be required, or credit any overpayment to Deposit Account No. 13-4771.

☒ This sheet is submitted in **duplicate**.

This transmittal letter has 2 total pages.

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DATE

Charles W. Bethards 36,453
Charles W. Bethards REG. NO.

Motorola, Inc.
Customer Number: 23330

Attorney of Record
Telephone No.: (480) 441-4237
Facsimile No.: (480) 441-5220

MISMATCH MODELING TOOL

Field of the Invention

This invention relates to mismatch models, and more particularly, to a mismatch calculator tool for predicting transistor, resistor and capacitor mismatch resulting from various conditions.

Background of the Invention

Mismatch is a leading cause of yield loss and a determining factor of circuit performance in analog, mixed-signal (AMS) ICs. A new method of modeling mismatch that accounts for variations in physical process parameters and is accurate over geometry and bias has been developed. However, as with prior mismatch models, the use of this new mismatch model required intensive manual calculations thus making it non-user friendly. Therefore, the application of the new mismatch methodology, or model, has been combined with computer programming and electronic circuit simulation and modeling resulting in a mismatch tool. Thus, users of the mismatch tool, such as designers and other engineering

professionals, can create more robust designs by quickly evaluating the mismatch opportunity in a fraction of the time that the manual calculations required and with more accuracy. The mismatch tool further allows the designer to simulate a variety of bias and geometry conditions in a matter of seconds, including providing batch-mode capability to perform multiple sweeps over bias and geometry to aid in finding a desired configuration.

Brief Description of the Drawings

FIG. 1 is a simplified functional block diagram of the mismatch modeling tool in an embodiment in accordance with the present invention;

FIG. 2 is an example of an interface to the mismatch modeling tool in an embodiment of the present invention;

FIG. 3 is a data entry input frame of the interface shown in FIG. 2;

FIG. 4 is a mismatch results output frame of the interface shown in FIG. 2 for a voltage driven scenario;

FIG. 5 is a mismatch results output frame of the interface shown in FIG. 2 for a current mirror scenario;

FIG. 6 is a mismatch results output frame of the interface shown in FIG. 2 for a differential pair scenario;

FIG. 7 shows an example of a mismatch results three dimensional output plot showing a sweet spot in a plot of Id versus geometry for an nmos current mirror;

FIG. 8 is the interface screen of FIG. 2 showing the data entry input frame and mismatch results output frame for a resistor mismatch calculation scenario;

FIG. 9 is the interface screen of FIG. 2 showing the data entry input frame and mismatch results output frame for a capacitor mismatch calculation scenario.

Detailed Description of the Drawings

Referring to FIG. 1, a simplified functional block diagram of a mismatch modeling tool 10 in an embodiment in accordance with the present invention is shown (the "mismatch tool 10" hereinafter). The mismatch tool 10 comprises the mismatch model $\sigma^2_{Id} = \Sigma(\partial I_d/\partial p_j)^2\sigma^2_{pj}$ ("mismatch model 30" hereinafter). The derivation and explanation of the mismatch model 30 is contained within the paper A Comprehensive MOSFET Mismatch Model by P. Drennan and C. McAndrew, IEEE ICMTS, 2000

("Drennan et al." hereinafter), the contents of which are incorporated herein by reference. Further explanation of the model is contained within Integrated Circuit Device Mismatch Modeling and Characterization for Analog Circuit Design, - Ph.D. dissertation, Arizona State University, May 1999, by P. Drennan ("Drennan" hereinafter) which is also incorporated herein by reference.

Referring again to FIG. 1, the mismatch tool 10 further comprises the mismatch model software 32, which is run upon a computer, or server, 26. The computer 26 is electronically connected to a circuit simulation library and program 14. The circuit simulation library and program 14 may be comprised of any of the many electronic circuit modeling and simulation packages available. Some examples include the SPICE program developed by the University of California - Berkeley, but may also include PSPICE, MCSPICE, Saber, SmartSpice, etc. The circuit simulation library and program 14 is stored, and may be executed, at a host location 12. The host location 12 may be integral to the computer 26, or may also represent an unrelated computer or storage location. The mismatch tool 10 further comprises mismatch model data libraries 18, stored within a host location 16. The mismatch

model data libraries 18 comprise process parameter variables used within the model 30 to account for the physical parameters affecting mismatch. As in the previous case, the host location 16 may be storage within, or part of, the computer 26, or may also represent an unrelated computer or storage location.

The mismatch tool 10 further comprises the data input and data output interfaces that may be comprised of any data interface method or system. In one embodiment, a web based application is utilized. A web based application is an application that is downloaded from a computer network each time the application is run. The computer network may be either an in-house local area network, or intranet, or a large scale wide area network, or internet. The advantage is that the application can be run from any computer, either on a local area network or via a wide area network such as the world wide web, and the software is routinely upgraded and maintained by the hosting organization rather than each individual user. Additionally, the web based applications are not limited to conventional web browser applications such as Netscape. Other web based application systems or programs may be employed within the web based application concept

without departing from the spirit or scope of the present invention.

In an embodiment of the present invention, a graphical interface 22 is presented preferably upon a user host 20. The user host 20 may be a standalone computer, a time shared computer terminal, etc. Furthermore, an email interface 28 may also preferably reside upon a user host 24, which again may be a standalone computer, a time shared computer terminal, etc. The use of an email interface 28 upon a separate host 24, connected electronically to the computer 26, allows remote users to submit and receive data from locations remote from the computer 26, including globally. The automated combination of the mismatch model 30, the mismatch model software 32, the circuit simulation library and program 14, and the mismatch model data libraries 18, gives users a significant advantage in achieving reduced cycle time for design and improved product quality through more robust designs.

The mismatch tool 10 in an embodiment of the present invention further comprises a plurality of different calculation scenarios: a Voltage Driven scenario, a Current Mirror scenario, and a Differential Pair scenario, for MOSFET

and BJT transistor devices; and a resistor calculation scenario and capacitor calculation scenario. Each of these calculation scenarios can be combined with calculations for other analog design objectives. Those skilled in the art will recognize that additional calculation scenarios other than these five are possible, and are also within the spirit and scope of the present invention. The five scenarios above are presented as examples of scenarios popular with those skilled in the art.

Referring to FIG. 2, an example of an interface to the mismatch tool 10 in an embodiment of the present invention is shown. The interface screen 100 comprises three major areas, or frames, in an embodiment of the present invention. The frames of the interface screen 100 comprise a calculation setup frame 110, a data input frame 130, and a data output frame 150. The data output frame 150 also comprises a message frame 158.

The frames of the interface screen 100 provide a user with the means to input data and receive returned output data in a graphical user friendly format. The user is guided through a sequence of pulldown menus within the calculation setup frame 110, wherein the user is presented with a

technology selection 112, a device type selection 114, a subtype selection 116 and a calculation type selection 118. Each of the pulldown menus is actively generated, using programming languages such as JavaScript, Perl, etc., based upon the preceding menu selections.

As new technologies are developed and added into an embodiment of the present invention, the programming and database libraries are modified to include data files comprising the added technology name along with its shrink factor and design unit information. These programming modifications make the technology available on the pull down menus in the calculation setup frame 110. Additionally, a technology directory (not shown herein) is also created that comprises the device types available for analysis. Included in this technology directory is an electronic circuit / component model file for insertion into the circuit simulation library and program 14 that is used for the simulations along with files of measured data to be used in the calculation for the variance and gradient terms, and new model data to be added into the mismatch model data libraries 18. The aforementioned programming changes may be

accomplished in a variety of methods by those skilled in the art.

The calculation setup frame 110 further comprises a View Related Plots 122 button, or link, that will launch a second graphical displaying a page that contains mismatch measured data, playback plots, and 3D and contour plots of the device mismatch over geometry, such as the 3D plot of Current Mirror mismatch versus geometry in FIG. 7. These plots help guide the user to opportunities for better mismatch, such as the sweet spot 210 shown on the right side of FIG. 7, that may otherwise not be apparent from single point solutions calculated in the mismatch tool 10.

Following the selection of the desired technology in the calculation setup frame 110, the user selects a create data entry input form 120 button. This selection causes the data input frame 130 to be generated.

Referring to FIG. 3, a data entry input frame 130 of the interface of FIG. 2 is shown. In an example of an embodiment of the present invention, an electronic circuit simulation model file name, it's revision number, and such other information as desired, is displayed at the top of the data entry input frame 130. The data entry input frame 130

further comprises geometry, bias and temperature condition selection parameters 132 for the selected technology and device. The specific geometry, bias and temperature condition parameters 132 that are generated following the selection of the create data entry input form 120 button are dependent upon the previous technology and device selections and therefore may vary. For example, the specific geometry, bias and temperature condition parameters 132 shown here in FIG. 3 result from the voltage driven scenario. However, additional or fewer fields may be generated for other scenarios, e.g. the current mirror and differential pair scenarios will also have a field, Np1, etc. to designate the number of devices placed in parallel. Those skilled in the art will be familiar with the bias and geometry condition parameters 132 displayed however. The user will next enter the desired bias, geometry and temperature values into the data entry fields reflecting the number of values desired for each parameter. The data entry fields are comprised of three columns: a single-value data entry column 126, a string-of-values data entry column 128, and range-of-value data entry column 138. Each of these data entry fields is utilized as follows. The single-value data entry column 126 accepts

single values for each geometry, bias and temperature condition parameter. The string-of-values data entry column 128 accepts a delimited list of values for each geometry, bias and temperature condition parameter. The range-of-value data entry column 138 allow the user to input sweeps of geometry, bias and temperature condition parameters by specifying the start, stop, and step values.

In one embodiment, the desired values for each geometry, bias and temperature condition parameter may be entered into the single-value data entry column 126, the string-of-values data entry column 128, and the range-of-value data entry column 138 in any combination of the three columns. If multiple columns contain data entries for the same geometry, bias and temperature condition parameters, the calculation precedence is established from right to left (i.e. the range-of-value data entry column 138 supercedes the string-of-values data entry column 128 which in turn supercedes the single-value data entry column 126.

Additionally, if the data input frame 130 contains values only in the single-value data entry column 126, the output is directed to the data output frame 150 shown on the right side of FIG.2, as well as in Figs 4-6. If either the

string-of-values data entry column 128, or the range-of-value data entry column 138 contains data, the output will be placed in a delimited text file (such as is suitable for importing into spreadsheet or word processing programs) and the user receives the results following the completion of the calculations. This feature is present since many applications, including web browsers such as Netscape, will time-out before the mismatch calculator 10 can return the results from multiple calculations to the data output frame 150. Also, since the multiple calculations can require a period of time to run, this feature allows the user to continue with other tasks while the calculations are being run. The comma delimited text file data table can be used to generate mismatch plots such the one in FIG. 7, to build behavioral models, for use as a look-up table, to generate trend plots over bias, geometry or temperature, and to compare devices within and across technologies. Fig 7 shows an example of a mismatch results three dimensional output plot showing a sweet spot 210 in a plot of Id versus geometry for an nmos current mirror.

An additional feature in an embodiment is that each of the parameter names, as well as any other desired label, may be hypertext linked to a short description or definition.

It should be noted that in an embodiment, the temperature condition parameter changes the operating temperature of the electronic circuit simulation package, such as SPICE, behind the mismatch tool 10 without the mismatch being measured and characterized over various temperatures. Changes in the temperature condition parameter will result in changes to the drain currents obtained from the SPICE simulation. In another embodiment of the present invention however, the mismatch may be measured and characterized over various temperatures.

An additional feature in an embodiment of the present invention is active error checking that automatically checks all bias and geometry condition parameter data entry values entered into the input columns: single-value data entry column 126, string-of-values data entry column 128, and/or range-of-value data entry column 138.

Below the input columns for geometry, bias and temperature, the user can choose to simulate the mismatch pair in a cross-couple configuration by entering appropriate

data values into cross-coupled configuration data entry fields 134 that are comprised of fields for Center-to-center and Sigmas(#). A cross-coupled pair is distinguished from a common centroid pair in that not all cross-coupled pairs are common centroid. That is, the effective center of the first device needs to be coincident with the effective center of the second device to be considered a common centroid pair.

In an embodiment of the present invention the user may also optionally select to show mismatch process parameter contributions, show capacitances, and show VdSat by selecting the appropriate Show Parameter checkboxes 136.

During the course of entering the above data, the user may reset all the fields to their default values by clicking on a reset button 124.

Once the user has entered all of the desired data input values, they then press a Calculate button 122. All of the user data that has been input into the data entry input frame 130 is collected and combined with information to form a SPICE or Mica type netlist. The netlist is run on the computer 26 and the results are parsed out to several variables. The simulation results are combined with the mismatch model 30 coefficients to perform the mismatch

calculations. A further feature of an embodiment of the present invention is the ability of the mismatch tool 10, using the mismatch model 30, to predict the mismatch standard deviation of a radially dependent gradient. Radially dependent gradients may result from spin-coat processes such as photoresist and developer deposition, or other single wafer process steps such as etch or material deposition. In the presence of radially dependant gradients, the matched pair of devices on one side of a wafer may have a positive gradient offset, while the matched pair on the opposite side of the wafer has a negative gradient offset. The overall measured distribution will still be centered about zero in the presence of the radial gradient, but the dispersion will bloom. Radial based gradients can be eliminated by using common centroid matched pairs. Thus, the mismatch tool 10 using the mismatch model 30, to predict the mismatch standard deviation of a radially dependent gradient is valid for common centroided pairs.

Referring again to FIG. 2, it will be recalled that the user is presented with the calculation type selection 118. This selection features five of the most popular types of

calculation scenarios for MOSFET and BJT transistors, resistors and capacitors as follows:

Voltage Driven Scenario

The Voltage Driven scenario was developed primarily for characterization and technology development engineers. Referring to FIG. 4, the entries for the Voltage Driven configuration in the calculation type selection 118 comprise: Vd - drain voltage; Vg - gate voltage; Vb - bulk; W - Width; and L - Length as are shown in the entered data frame 152a.

Continuing with FIG. 4, a data output frame 150a is shown. The data output frame 150a contains two columns of data. The Id mismatch 154a, presented in the left column, is given as a percent difference between two devices. The right column contains the Vg mismatch 155a, which is the input offset voltage.

The first row of output data is the total Id and Vg mismatch 157a, given as a one-sigma standard deviation number, although this is user definable. The (+/-) notation indicates that the distribution is symmetric and that this offset number is for one side of the distribution. A total mismatch is computed from the individual process parameter contributions listed in the remaining rows of data parameters

159a comprised of: dl - offset in polysilicon gate length; dwox - offset in active region width; gox - gate oxide thickness; nsub - substrate dopant concentration; rsh - source and drain sheet resistances; ubref - reference mobility; vfb - flatband voltage; vtl - modification of Vfb for short channel devices, and Vtw - accounts for changes in MOSFET narrow-width and inverse-narrow-width effects.

All process parameter contributions are given as one-sigma standard deviation numbers and these parameters are combined as a root-sum-of-squares to generate the total mismatch 157a (i.e. square each standard deviation to get a variance, add the variances, and square-root the total variance to the total standard deviation.) The user, by examining the data parameters 159a results that are presented in the data output frame 150a, will be able to determine the major contributors to the mismatch in a particular case. The user can then use this information to target those parameters that affect the mismatch.

Current Mirror Scenario

The Current Mirror mismatch scenario was developed primarily for analog and mixed-signal designers although many designers will find the mismatch tool 10 of value. The

entries for the Current Mirror configuration entries into the calculation type selection 118 comprise: Vd - drain voltage; Vb - bulk; Iref - reference current; W - Width; and L - Length as are shown in the entered data frame 152b depicted in FIG. 5.

The Current Mirror scenario differs from the Voltage Driven scenario in that the user has the option of specifying the number of unit devices placed in parallel, Np1 and Np2, for both M_1 and M_2 through the use of an additional data entry field in the data input frame 130 (not shown in FIG. 2). This makes the mismatch tool 10 suitable for simulating the mismatch in the presence of ratioed mirrors. The variances across each of the unit devices, in a grouping of parallel devices, add to give the total variance. But, the overall sensitivity of the mirror to each unit device is reduced, thereby giving an overall reduction in mismatch when multiple devices are placed in parallel.

Referring to FIG. 5, a differential pair scenario assumes a particular circuit. As an aide to the user, the message frame 158 will display that circuit. Thus - message frame 158 shows a picture of the assumed circuit 158a.

An example mismatch tool 10 output frame 150b depicted in FIG. 5, contains two columns of data, the Total mismatch 154b, and the mismatch without the output conductance, go, on M_2, w/o go on M2 155b. In the latter case, w/o go on M2 155b, the mismatch simulation is performed with the drain of M_1 tied to the gate of M_2. In this manner, the mismatch results can be added to a SPICE TYPE circuit netlist without double counting the effect of the output conductance on M_2.

A total mismatch 157b is computed from the individual process parameter contributions listed in the remaining rows of data parameters 159b comprised of: dl - offset in polysilicon gate length; dwox - offset in active region width; gox - gate oxide thickness; nl - substrate dopant concentration; rsh - source and drain sheet resistances; ubref - reference mobility; vfb - flatband voltage; and vtl - modification of Vfb for short channel devices.

As in the voltage driven scenario, all process parameter contributions are given as one-sigma standard deviation numbers, that may be user defined to other than one-sigma, and these parameters are combined as a root-sum-of-squares to generate the total mismatch 157b. The user, by examining the data parameters 159b results that are presented in the data

output frame 150b, will be able to determine the major contributors to the mismatch in a particular case. The user can then use this information to target those parameters that affect the mismatch.

Since Current Mirrors are often operated over a range of current, the mismatch can change dramatically over the operating region of the matched pair (approximately 5X in this case). The mismatch tool 10 allows the user to sweep the bias conditions to check the mismatch over the anticipated operating region.

Note that Vg mismatch is not provided for the Current Mirror case since the gates of M_1 and M_2 are tied together and cannot be offset. For this requirement, the current driven, Differential Pair scenario is suggested.

Differential Pair Scenario

The Differential Pair scenario depicted in FIG. 6 was also developed primarily for analog and mixed-signal designers although again many designers will find the mismatch tool 10 of value. The Differential Pair scenario is nearly identical to the Voltage Driven scenario with the exception that the MOSFET matched pair is current driven. The entries for the Differential Pair configuration entries

into the calculation type selection 118 comprise: Iref - reference current (Iref for the Differential Pair is the current for both branches; Data Entered into interface for p-type must be entered as a negative i.e. -10u); Vd - drain voltage; Vb - bulk; W - Width; and L - Length as are shown in the entered data frame 152c. An additional data entry field in the data input frame 130 (not shown in FIG. 2) allows the user to change the number of devices placed in parallel which is required to be the same for both the left and right devices.

Referring to FIG. 6, a differential pair scenario assumes a particular circuit. As an aide to the user, the message frame 158 will display that circuit. Thus - message frame 158 shows a picture of the assumed circuit 158b.

Referring further to FIG. 6, the data output frame 150c is shown. The data output frame 150c contains two columns of data. The Id mismatch 154c, presented in the left column, is given as a percent difference between two devices. The right column contains the Vg mismatch 155c, which is the input offset voltage.

The first row of output data is the total Id and Vg mismatch 157c, again, given as a one-sigma standard deviation

number that may be user defined to other than one-sigma. The (+/-) notation indicates that the distribution is symmetric and that this offset number is for one side of the distribution. A total mismatch is computed from the individual process parameter contributions listed in the remaining rows of data parameters 159c comprised of: dl - offset in polysilicon gate length; dwox - offset in active region width; gox - gate oxide thickness; nsub - substrate dopant concentration; rsh - source and drain sheet resistances; ubref - reference mobility; vfb - flatband voltage; vtl - modification of Vfb for short channel devices, and Vtw - accounts for changes in MOSFET narrow-width and inverse-narrow-width effects.

The user, by examining the data parameters 159c results that are presented in the data output frame 150c, will be able to determine the major contributors to the mismatch in a particular case. The user can then use this information to target those parameters that affect the mismatch.

Referring to FIG. 7, an example of a mismatch results three dimensional output plot showing a sweet spot in a plot of Id versus geometry for an nmos current mirror ("output plot 200" hereinafter) is shown. The example output plot 200

shows the results of a spread or range of calculations such as would have been input into the string-of-values data entry column 128 or the range-of-value data entry column 138. Thus - the user when presented with an output plot 200 as shown can immediately discern the sweet spot 210.

Mismatch variance is not the only design objective for a matched pair of devices. Thus - an embodiment of the present invention has as further features the addition of several parameter calculations to the mismatch tool 10 to allow simultaneous monitoring of multiple criteria. With every circuit configuration, as previously discussed, the nominal Id is provided. For the Current Mirror and the Differential Pair scenarios of FIG. 5 and 6, the nominal Vg, is provided and the Current Mirror scenario output reports Id/I ref.

Resistor Scenario

Referring to FIG. 8, an interface screen showing the data entry input frame and mismatch results output frame for a resistor mismatch calculation scenario is shown. The interface screen 100, as previously discussed, comprises a calculation setup frame 110, a data input frame 130, a data output frame 150, and a message frame 158. In the resistor

calculation scenario in an embodiment of the present invention, the user will select a device type selection 114 designating a resistor (abbreviated "RES" in FIG. 8. Following completion of the selections of the desired technology and the create data entry input form 120 button in the calculation setup frame 110, the data input frame 130 is generated.

The data entry input frame 130 comprises length and width selection parameters 132. The specific length and width parameters 132 that are generated following the selection of the create data entry input form 120 button are dependent upon the previous technology and device selections and therefore may vary. As previously discussed, the desired values for the width and length parameters may be entered into the single-value data entry column 126, the string-of-values data entry column 128, and the range-of-value data entry column 138 in any combination of the three columns. And as before, if multiple columns contain data entries for the same width and length parameters, the calculation precedence is established from right to left (i.e. the range-of-value data entry column 138 supercedes the string-of-

values data entry column 128 which in turn supercedes the single-value data entry column 126.

Below the input columns for width and length, the user can choose to simulate the mismatch pair in a cross-couple configuration by entering appropriate data values into cross-coupled configuration data entry fields 134 that are comprised of fields for Center-to-center and Sigmas(#). It should be noted that the process for computing the mismatch is a little different for the resistor scenario then that of the transistor scenarios. The primary difference is that a SPICE or MCSPICE type program is not utilized as the calculation is much simpler. Instead, a parameter file is used for the measured data terms.

An additional difference is the equation for computing the mismatch. The computational code for this mismatch calculation is: $(\sigma_C^2/C^2) = (\sigma_L^2/L^2) + (\sigma_w^2/W^2) + (\sigma_{LW}^2/LW) + (g*ctc^2)$.

Following the calculation of the resistor scenario, if the data input frame 130 contains values only in the single-value data entry column 126, the output is directed to the data output frame 150. And as previously discussed, if

either the string-of-values data entry column 128, or the range-of-value data entry column 138 contains data, the output will be placed in a delimited text file (such as is suitable for importing into spreadsheet or word processing programs) and the user receives the results following the completion of the calculations.

The data output frame 150d contains one column of data showing the percent difference between devices given as a one-sigma standard deviation number, although this is user definable. All process parameter contributions are given as one-sigma standard deviation numbers and these parameters are combined as a root-sum-of-squares to generate the total mismatch 162. As before, the (+/-) notation indicates that the distribution is symmetric and that this offset number is for one side of the distribution.

Capacitor Scenario

Referring to FIG. 9, an interface screen showing the data entry input frame and mismatch results output frame for a capacitor mismatch calculation scenario is shown. The interface screen 100, as previously discussed, comprises a calculation setup frame 110, a data input frame 130, a data output frame 150, and a message frame 158. In the capacitor

calculation scenario embodiment, the user will select a device type selection 114 designating a capacitor (abbreviated "CAP" in FIG. 9. Following completion of the selections of the desired technology and the create data entry input form 120 button in the calculation setup frame 110, the data input frame 130 is generated.

The data entry input frame 130 comprises length and width selection parameters 132. The specific length and width parameters 132 that are generated following the selection of the create data entry input form 120 button are dependent upon the previous technology and device selections and therefore may vary. As previously discussed, the desired values for the width and length parameters may be entered into the single-value data entry column 126, the string-of-values data entry column 128, and the range-of-value data entry column 138 in any combination of the three columns. And as before, if multiple columns contain data entries for the same width and length parameters, the calculation precedence is established from right to left (i.e. the range-of-value data entry column 138 supercedes the string-of-values data entry column 128 which in turn supercedes the single-value data entry column 126.

Below the input columns for width and length, the user can choose to simulate the mismatch pair in a cross-couple configuration by entering appropriate data values into cross-coupled configuration data entry fields 134 that are comprised of fields for Center-to-center and Sigmas(#). It should be noted that the process for computing the mismatch is a little different for the capacitor scenario then that of the transistor scenarios. The primary difference is that a SPICE or MCSPICE type program is not utilized as the calculation is much simpler. Instead, a parameter file is used for the measured data terms.

An additional difference is the equation for computing the mismatch. The computational code for this mismatch calculation is:

$$(\sigma_C^2/C^2) = (\sigma_L^2/L^2) + (\sigma_w^2/W^2) + (\sigma_{LW}^2/LW) + (g*ctc^2) .$$

Following the calculation of the capacitor scenario, if the data input frame 130 contains values only in the single-value data entry column 126, the output is directed to the data output frame 150. And as previously discussed, if either the string-of-values data entry column 128, or the range-of-value data entry column 138 contains data, the output will be placed in a delimited text file (such as is

suitable for importing into spreadsheet or word processing programs) and the user receives the results following the completion of the calculations.

The data output frame 150e contains one column of data showing the percent difference between devices given as a one-sigma standard deviation number, although this is user definable. All process parameter contributions are given as one-sigma standard deviation numbers and these parameters are combined as a root-sum-of-squares to generate the total mismatch 162. As before, the (+/-) notation indicates that the distribution is symmetric and that this offset number is for one side of the distribution.

While the invention has been particularly shown and described with reference to the embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form, and details may be made therein without departing from the spirit and scope of the invention.

WHAT IS CLAIMED IS:

1. A mismatch modeling tool comprising:

a software implemented transistor mismatch model;

at least one editable mismatch model data library comprising process parameter variables accessed by said software implemented transistor mismatch model;

a circuit simulation library and program data output accessed by said software implemented transistor mismatch model; and

a graphical interface to said software implemented transistor mismatch model.

2. The mismatch modeling tool of Claim 1 wherein said graphical interface comprises a menu driven modeled device selection frame.

3. The mismatch modeling tool of Claim 2 wherein said menu driven modeled device selection frame configures said software implemented transistor mismatch model to display a dynamically generated input data frame within said graphical interface.

4. The mismatch modeling tool of Claim 3 wherein said dynamically generated input data frame reflects data input fields of one of a plurality of input scenarios comprising at least one of:

a voltage driven scenario;

a current driven scenario;

a differential pair scenario;

a resistor scenario; and

a capacitor scenario.

5. The mismatch modeling tool of Claim 4 wherein said dynamically generated input data frame comprises a plurality of data input columns comprised of at least one of:

a plurality of single-data input parameter fields;

a plurality of string-of-data input parameter fields; and

a plurality of range-of-data input parameter fields.

6. The mismatch modeling tool of Claim 5 further comprising an electronically transmitted ASCII output data file, said ASCII output data file comprising output data reflecting at least one of:

said plurality of single-data input parameter fields;

said plurality of string-of-data input parameter fields; and

said plurality of range-of-data input parameter fields.

7. The mismatch modeling tool of Claim 6 wherein said ASCII output data file is an emailed ASCII output data file.

8. The mismatch modeling tool of Claim 6 further comprising a three dimensional output plot, said three dimensional output plot being a graphical representation of said output data within said ASCII output data file.

9. The mismatch modeling tool of Claim 5 further comprising a dynamically generated output data frame, said dynamically generated output data frame displaying output data reflecting said plurality of single-data input parameter fields.

10. A mismatch modeling tool comprising:

a software implemented transistor mismatch model;

at least one editable mismatch model data library comprising process parameter variables accessed by said software implemented transistor mismatch model; and

a circuit simulation library and program data output accessed by said software implemented transistor mismatch model.

11. The mismatch modeling tool of Claim 10 further comprising a graphical interface to said software implemented transistor mismatch model.

12. The mismatch modeling tool of Claim 11 wherein said software implemented transistor mismatch model is configurable for a plurality of input scenarios comprising at least one of:

a voltage driven scenario;

a current driven scenario;

a differential pair scenario;

a resistor scenario; and

a capacitor scenario.

13. The mismatch modeling tool of Claim 12 wherein said graphical interface comprises a dynamically generated input data frame, said dynamically generated input data frame displaying parameters reflecting a selected said input scenario.

14. The mismatch modeling tool of Claim 13 wherein said dynamically generated input data frame comprises a plurality of data input columns comprised of at least one of:

a plurality of single-data input parameter fields;

a plurality of string-of-data input parameter fields; and

a plurality of range-of-data input parameter fields.

15. The mismatch modeling tool of Claim 14 further comprising a dynamically generated output data frame, said dynamically generated output data frame displaying output data reflecting said plurality of single-data input parameter fields.

16. The mismatch modeling tool of Claim 14 further comprising an electronically transmitted ASCII output data file, said ASCII output data file comprising output data reflecting at least one of:

said plurality of single-data input parameter fields;

said plurality of string-of-data input parameter fields; and

said plurality of range-of-data input parameter fields.

17. The mismatch modeling tool of Claim 16 further comprising a three dimensional output plot, said three dimensional output plot being a graphical representation of said output data within said ASCII output data file.

18. The mismatch modeling tool of Claim 13 wherein said dynamically generated input data frame comprises a plurality of data input columns comprised of at least one of:

a plurality of string-of-data input parameter fields; and

a plurality of range-of-data input parameter fields.

19. The mismatch modeling tool of Claim 18 further comprising an ASCII output data file, said ASCII output data file comprising output data reflecting at least one of:

said plurality of string-of-data input parameter fields; and

said plurality of range-of-data input parameter fields.

20. The mismatch modeling tool of Claim 19 further comprising a three dimensional output plot, said three dimensional output plot being a graphical representation of said output data within said ASCII output data file.

MISMATCH MODELING TOOL

ABSTRACT

A mismatch modeling tool (10) comprises a software implemented mismatch model (32). The software implemented mismatch model (32) accesses: at least one editable mismatch model data library (18) comprising process parameter variables, and circuit simulation library and program (14) data output. An interface screen (100) provides input and output coupling between a user and the software implemented mismatch model (32).

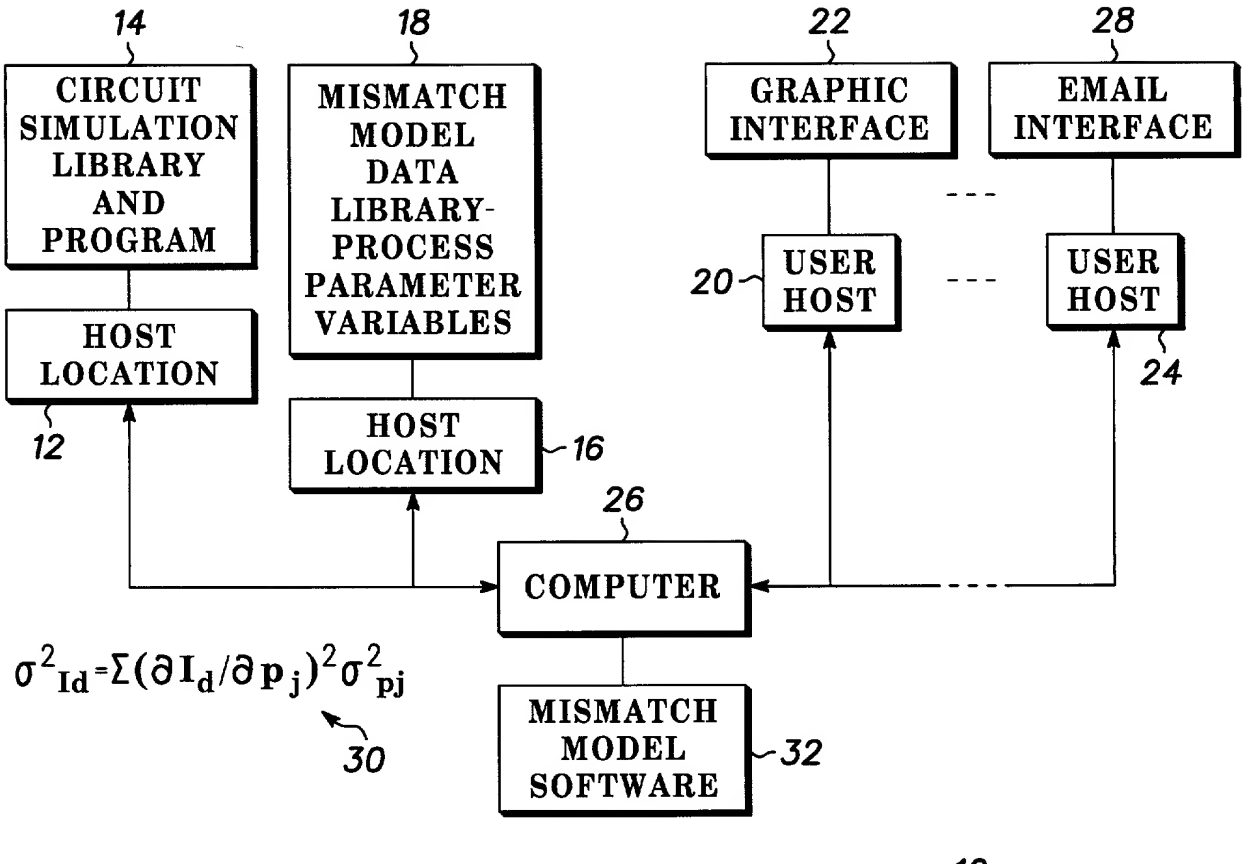

14
CIRCUIT SIMULATION LIBRARY AND PROGRAM
HOST LOCATION
12
18
MISMATCH MODEL DATA LIBRARY-PROCESS PARAMETER VARIABLES
HOST LOCATION
16
22
GRAPHIC INTERFACE
28
EMAIL INTERFACE
20
USER HOST
USER HOST
24
26
COMPUTER
$\sigma^2_{Id}=\Sigma(\partial I_d/\partial p_j)^2\sigma^2_{pj}$
30
MISMATCH MODEL SOFTWARE
32
10

FIG. 1

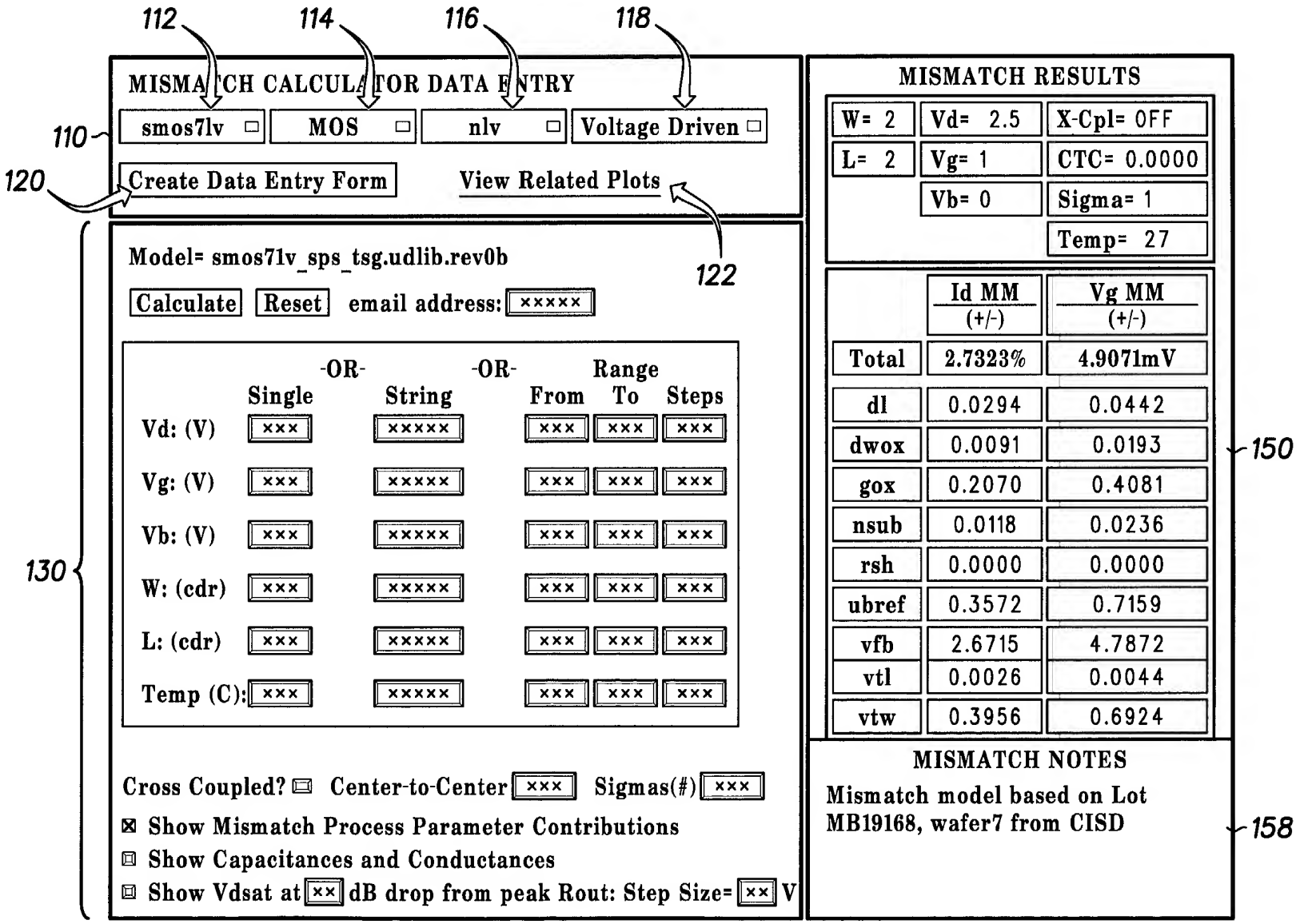
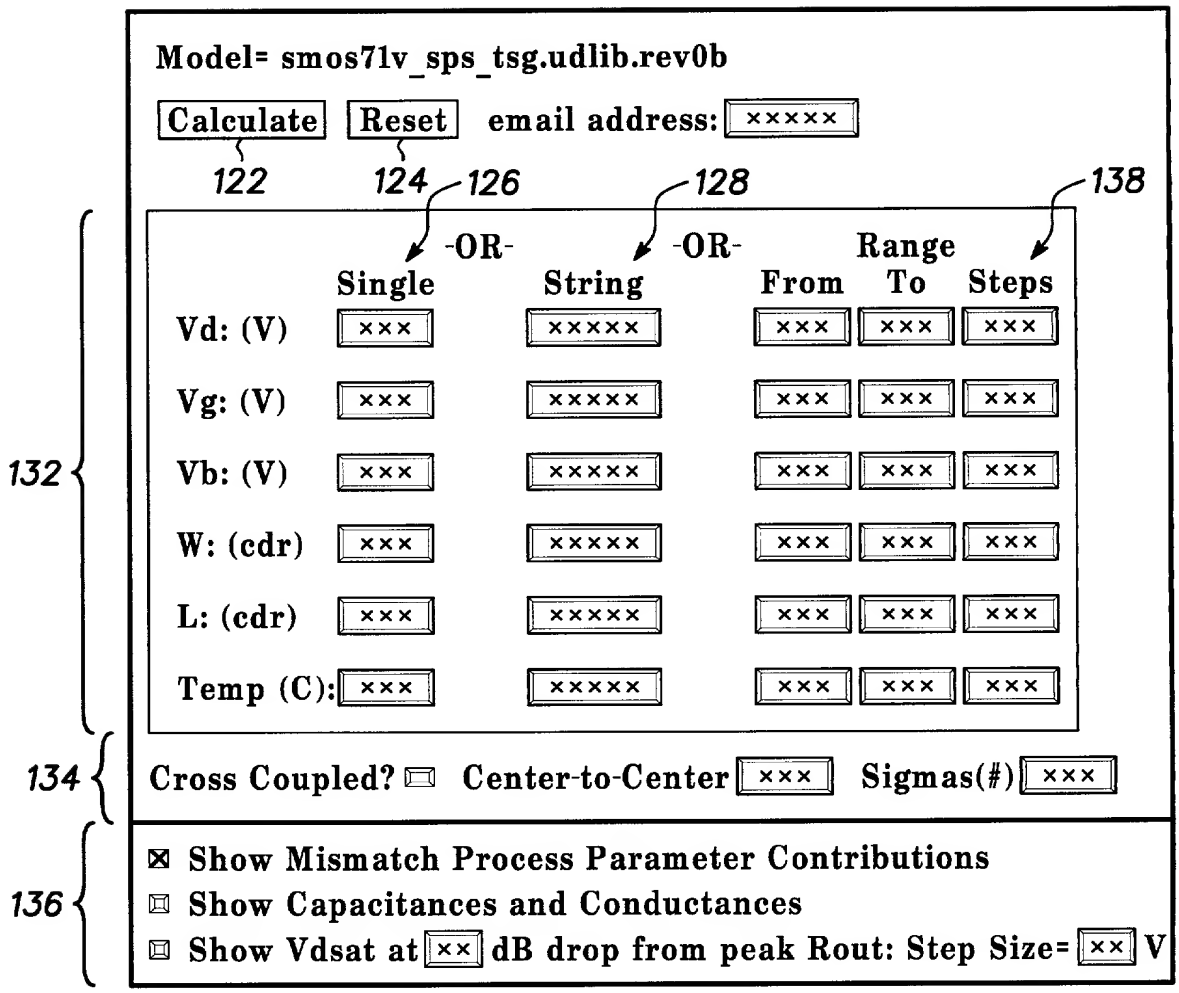

112
114
116
118
MISMATCH CALCULATOR DATA ENTRY
smos7lv
MOS
nlv
Voltage Driven
110
120
Create Data Entry Form
View Related Plots
122
Model= smos71v_sps_tsg.udlib.rev0b
Calculate
Reset
email address:
-OR-
-OR-
Range
Single
String
From
To
Steps
Vd: (V)
Vg: (V)
Vb: (V)
W: (cdr)
L: (cdr)
Temp (C):
130
Cross Coupled?
Center-to-Center
Sigmas(#)
Show Mismatch Process Parameter Contributions
Show Capacitances and Conductances
Show Vdsat at
dB drop from peak Rout: Step Size=
V
MISMATCH RESULTS
W= 2
Vd= 2.5
X-Cpl= OFF
L= 2
Vg= 1
CTC= 0.0000
Vb= 0
Sigma= 1
Temp= 27
Id MM (+/-)
Vg MM (+/-)
Total 2.7323% 4.9071mV
dl 0.0294 0.0442
dwox 0.0091 0.0193
gox 0.2070 0.4081
nsub 0.0118 0.0236
rsh 0.0000 0.0000
ubref 0.3572 0.7159
vfb 2.6715 4.7872
vtl 0.0026 0.0044
vtw 0.3956 0.6924
150
MISMATCH NOTES
Mismatch model based on Lot MB19168, wafer7 from CISD
158
100

FIG. 2


Model= smos71v_sps_tsg.udlib.rev0b
Calculate
Reset
email address: xxxxx
122
124
126
128
138
-OR-
-OR-
Range
Single
String
From
To
Steps
Vd: (V)
Vg: (V)
Vb: (V)
W: (cdr)
L: (cdr)
Temp (C):
xxx
xxxxx
132
134
Cross Coupled?
Center-to-Center
Sigmas(#)
136
Show Mismatch Process Parameter Contributions
Show Capacitances and Conductances
Show Vdsat at xx dB drop from peak Rout: Step Size= xx V

130

FIG. 3

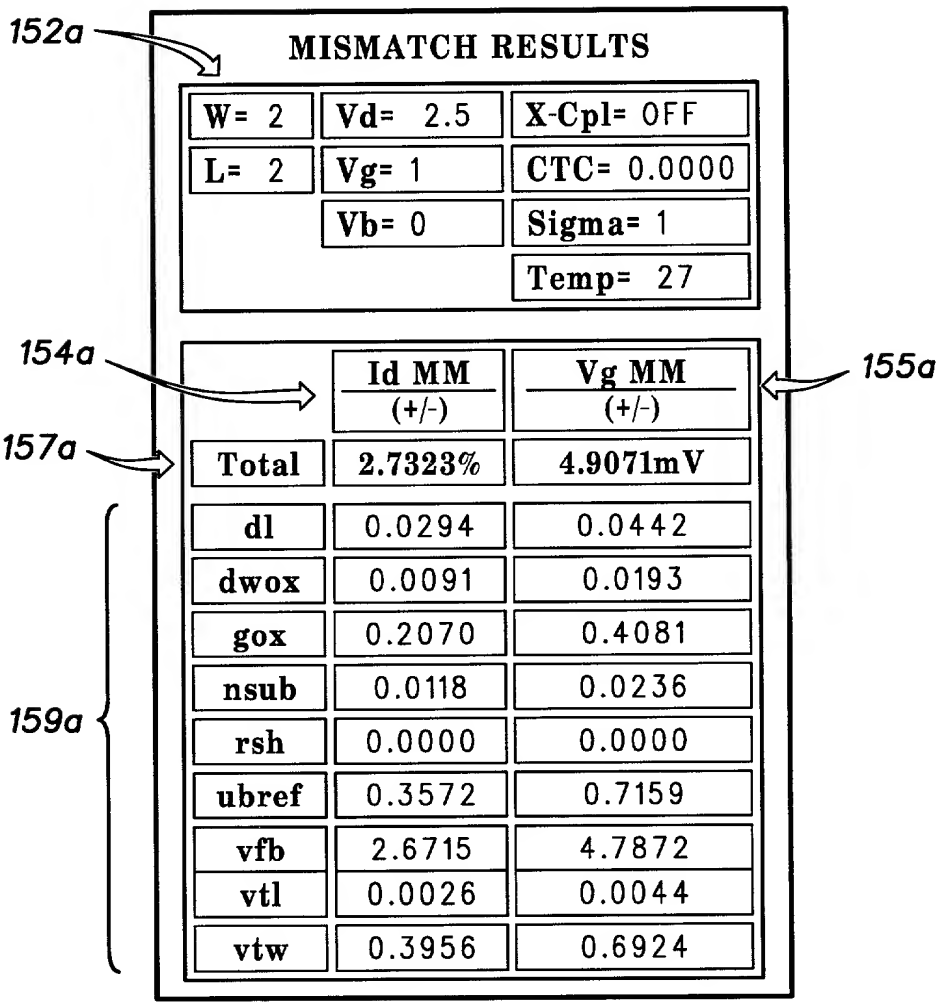

152a
MISMATCH RESULTS
W= 2
Vd= 2.5
X-Cpl= OFF
L= 2
Vg= 1
CTC= 0.0000
Vb= 0
Sigma= 1
Temp= 27
154a
155a
157a
159a
Id MM (+/-)
Vg MM (+/-)
Total
2.7323%
4.9071mV
dl 0.0294 0.0442
dwox 0.0091 0.0193
gox 0.2070 0.4081
nsub 0.0118 0.0236
rsh 0.0000 0.0000
ubref 0.3572 0.7159
vfb 2.6715 4.7872
vtl 0.0026 0.0044
vtw 0.3956 0.6924
150a

FIG. 4

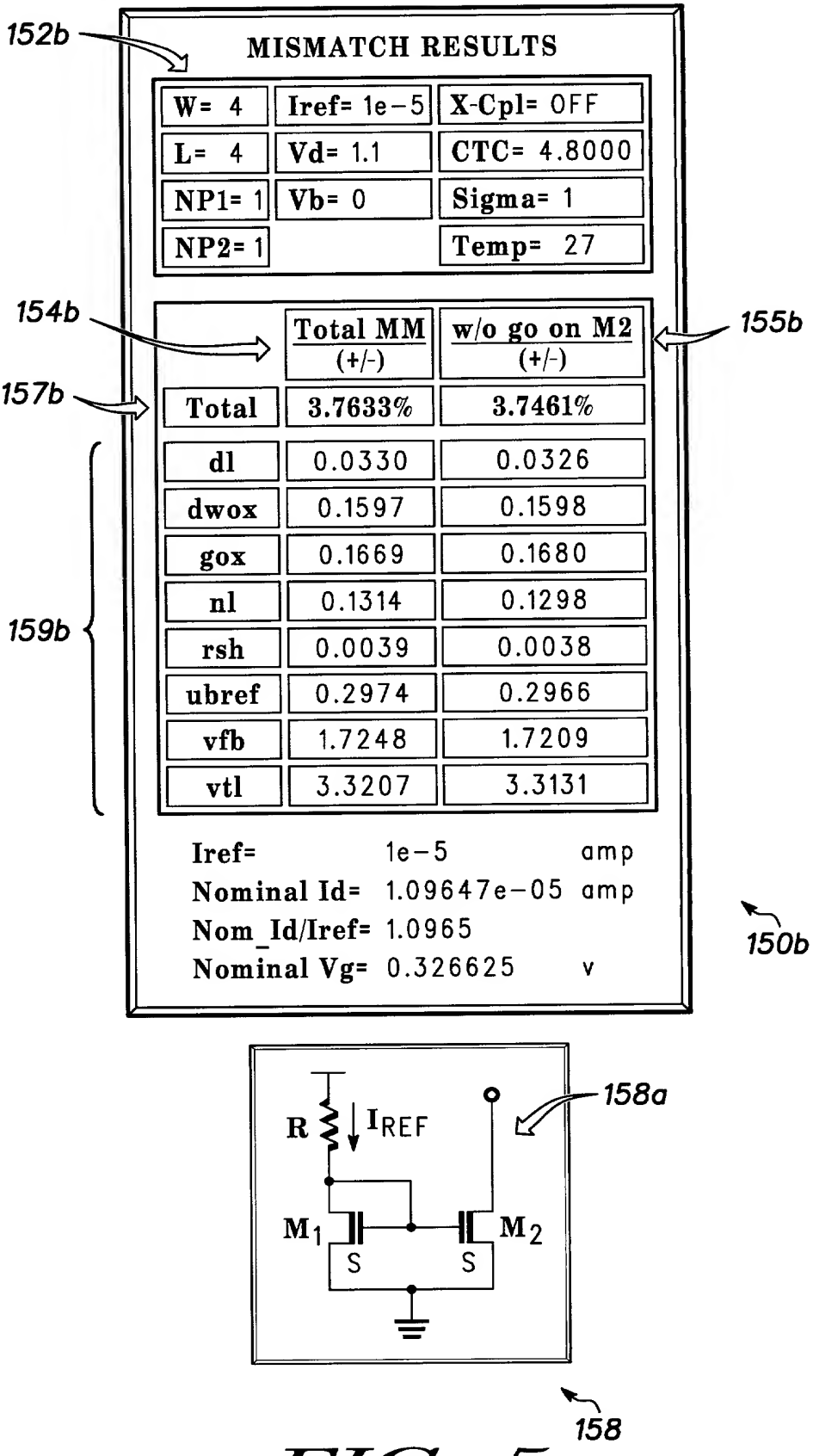

152b
MISMATCH RESULTS
W= 4
Iref= 1e-5
X-Cpl= OFF
L= 4
Vd= 1.1
CTC= 4.8000
NP1= 1
Vb= 0
Sigma= 1
NP2= 1
Temp= 27
154b
155b
157b
159b
Total MM (+/-)
w/o go on M2 (+/-)
Total 3.7633% 3.7461%
dl 0.0330 0.0326
dwox 0.1597 0.1598
gox 0.1669 0.1680
nl 0.1314 0.1298
rsh 0.0039 0.0038
ubref 0.2974 0.2966
vfb 1.7248 1.7209
vtl 3.3207 3.3131
Iref= 1e-5 amp
Nominal Id= 1.09647e-05 amp
Nom_Id/Iref= 1.0965
Nominal Vg= 0.326625 v
150b
R
IREF
158a
M1
M2
S
S
158

FIG. 5

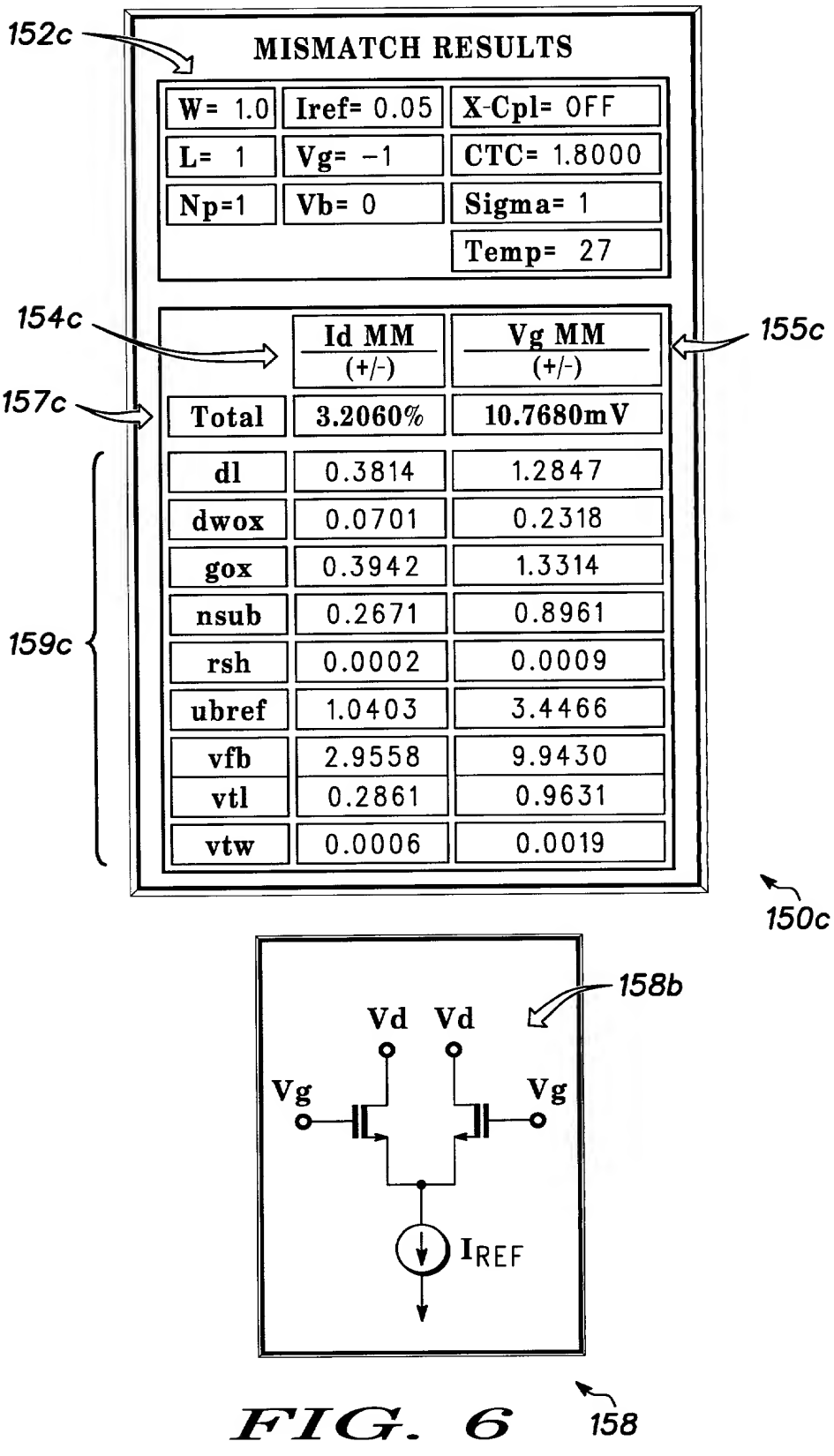
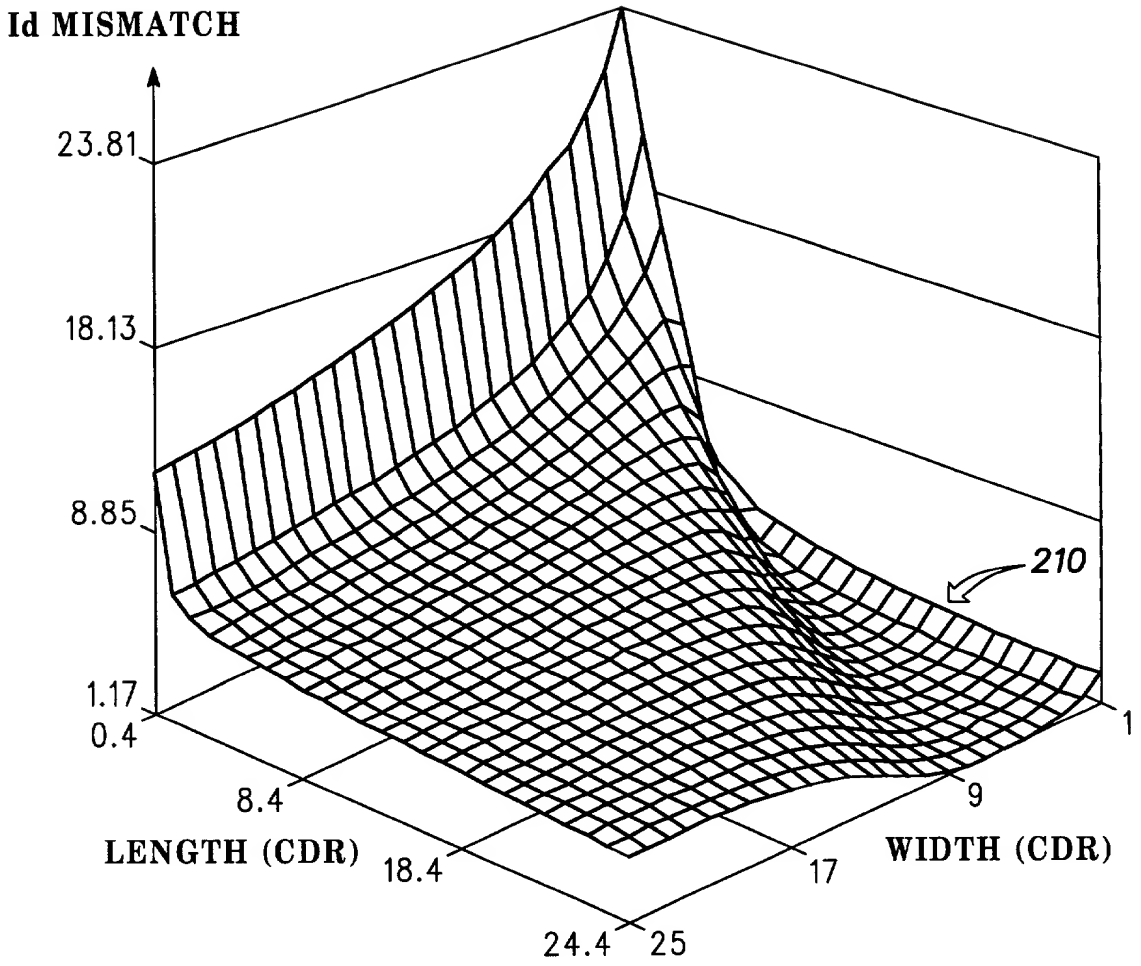

152c
MISMATCH RESULTS
W= 1.0
Iref= 0.05
X-Cpl= OFF
L= 1
Vg= −1
CTC= 1.8000
Np=1
Vb= 0
Sigma= 1
Temp= 27
154c
Id MM (+/-)
Vg MM (+/-)
155c
157c
Total
3.2060%
10.7680mV
dl 0.3814 1.2847
dwox 0.0701 0.2318
gox 0.3942 1.3314
nsub 0.2671 0.8961
rsh 0.0002 0.0009
ubref 1.0403 3.4466
vfb 2.9558 9.9430
vtl 0.2861 0.9631
vtw 0.0006 0.0019
159c
150c
158b
Vd Vd
Vg
Vg
IREF
158

FIG. 6


Id MISMATCH
23.81
18.13
8.85
1.17
0.4
8.4
18.4
24.4
LENGTH (CDR)
1
9
17
25
WIDTH (CDR)
210

200

FIG. 7

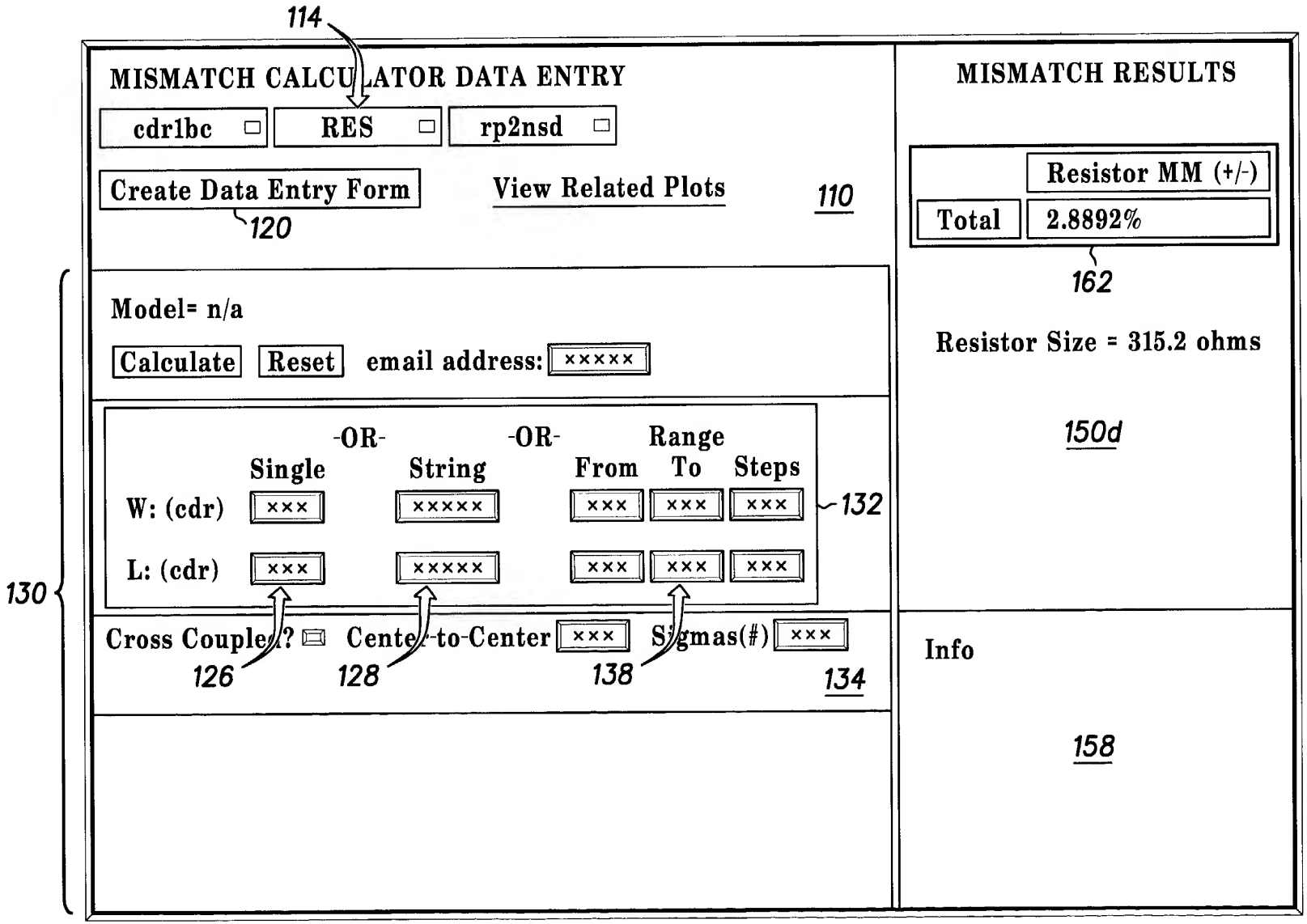

114
MISMATCH CALCULATOR DATA ENTRY
cdr1bc
RES
rp2nsd
Create Data Entry Form
120
View Related Plots
110
MISMATCH RESULTS
Resistor MM (+/-)
Total
2.8892%
162
Model= n/a
Calculate
Reset
email address:
xxxxx
-OR-
-OR-
Range
Single
String
From
To
Steps
W: (cdr)
L: (cdr)
xxx
xxxxx
132
130
Cross Coupled?
Center-to-Center
Sigmas(#)
126
128
138
134
150d
Info
158

FIG. 8

100

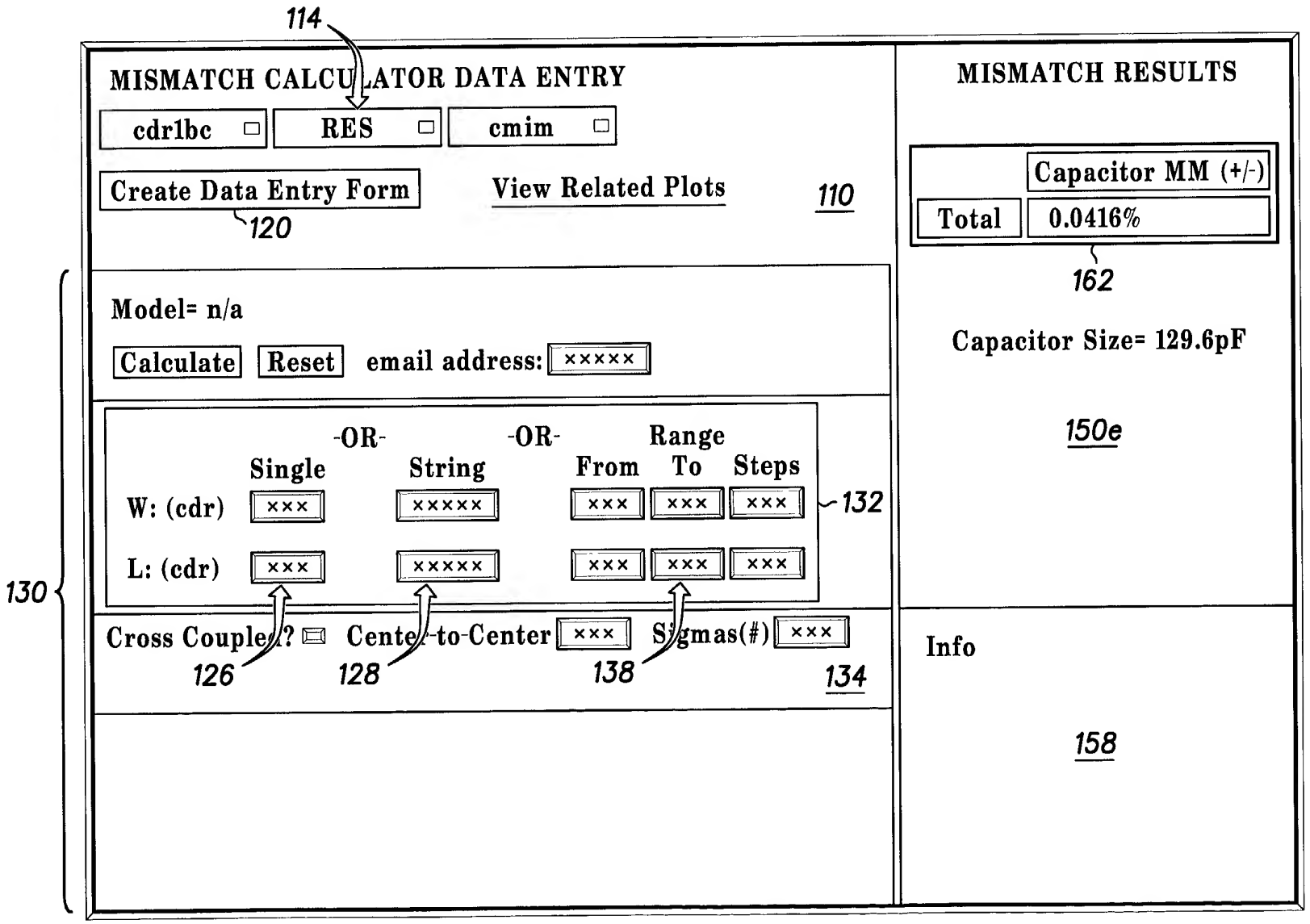

114
MISMATCH CALCULATOR DATA ENTRY
cdr1bc
RES
cmim
Create Data Entry Form
120
View Related Plots
110
MISMATCH RESULTS
Capacitor MM (+/-)
Total
0.0416%
162
Model= n/a
Calculate
Reset
email address:
xxxxx
-OR-
-OR-
Range
Single
String
From
To
Steps
W: (cdr)
L: (cdr)
xxx
xxxxx
132
130
Cross Coupled?
Center-to-Center
Sigmas(#)
126
128
138
134
Capacitor Size= 129.6pF
150e
Info
158
100

FIG. 9

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket SC11244ZC

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below), or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled MISMATCH MODELING TOOL, the specification of which is attached hereto unless the following box is checked:

☐ Application was filed on _____
as Application No. _____
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or 365(b) any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, § 119 of any United States provisional application(s), listed below:

_____ (Application Number)	_____ (Filing Date)
_____ (Application Number)	_____ (Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below:

(U.S. Parent Application Number or PCT Parent No.)	(Filing Date)	(Country)
(U.S. Parent Application Number or PCT Parent No.)	(Filing Date)	(Country)

I hereby appoint the attorney(s) and/or agent(s) associated with Customer Number 23330 to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Address all telephone calls to Mr. Charles W. Bethards at telephone no. (480) 441-4237.

Address all correspondence to customer number 23330.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF FIRST INVENTOR: FIRST MIDDLE LAST	INVENTOR'S SIGNATURE:	DATE: (SPELLOUT MONTH)
Cynthia L. Recker	Cynthia L. Recker	August 31, 2000
RESIDENCE:		CITIZENSHIP:
3819 East Ivyglen Street, Mesa, AZ 85205		United States
POST OFFICE ADDRESS:		
Same as above		

FULL NAME OF SECOND INVENTOR: FIRST MIDDLE LAST	INVENTOR'S SIGNATURE:	DATE: (SPELLOUT MONTH)
Patrick G. Drennan	Patrick G Drennan	August 31, 2000
RESIDENCE:		CITIZENSHIP:
961 West Juanita Avenue, Gilbert, AZ 85233		United States
POST OFFICE ADDRESS:		
Same as above		